CLAIMS

1. Coherence controller (64) adapted for being connected to a plurality of processors (40, 40') equipped with a cache memory (42, 42') and with at least one local main memory (44) in order to define a local module (50) of basic multiprocessors (60), said coherence controller (64) including a cache filter directory (84) comprising a first filter directory SF designed to guarantee coherence between the local main memory (44) and the cache memories (42, 42') of the local module, characterized in that it also includes an external port (99) adapted for being connected to at least one external multiprocessor module (51, 52, 53) identical to or compatible with said local module (50), the cache filter directory (84) including a complementary filter directory ED for keeping track of the coordinates, particularly the addresses, of the lines or blocks of the local main memory (44) copied from the local module (50) into an external module (51, 52, 53) and guaranteeing coherence between the local main memory (44) and the cache memories (42, 42') of the local module (50) and the external modules (51, 52, 53).

2. Coherence controller (64) according to claim 1, characterized in that it also includes an "n"-bit presence vector (86), where N is the number of basic multiprocessors in a module, an "N-1"-bit extension (88) of the presence vector, where N-1 is the total number of external modules (51, 52, 53) connected to the external port (99), and an Exclusive status bit (87).

3. Coherence controller (64) according to claim 2, characterized in that the external port (99) is connected directly or indirectly to the external modules (51, 52, 53) via an external two-point link (55).

4. Coherence controller (64) according to claim 2, characterized in that it includes "n" control units PU (80-83) of local ports (90-93) connected to the n basic multiprocessors (60-63) of the local module (50), a control unit XPU (89) of the external port (99) and a common control unit ILU of the filter directories SF/ED (84).

5. Coherence controller (64) according to claim 4, characterized in that the control unit XPU (89) of the external port and the control units PU (80-83) of the local ports are compatible with one another and use similar, largely common protocols.

6. Multiprocessor module (50), characterized in that it includes a plurality of multiprocessors (60-63) equipped with at least one cache memory (42, 42') and at least one main memory (44) and connected to a coherence controller (64) according to any of claims 1 through 5.

7. Multiprocessor system with a multimodule architecture, characterized in that it includes at least two multiprocessor modules (50-53) according to claim 6, connected to one another directly or indirectly through the external ports (99) of the coherence controllers (64).

8. Multiprocessor system according to claim 7, characterized in that said external ports (99) are connected to one another through a switching device or router (54).

9. Multiprocessor system according to claim 8, characterized in that the switching device or router (54) includes means for managing and/or filtering the data and/or requests in transit.

10. Large-scale symmetric multiprocessor server with a multimodule architecture characterized in that it comprises "N" multiprocessor modules (50-53) that are identical or compatible with one another, each module comprising a plurality of "n" basic multiprocessors (60-63) equipped with at least one cache memory (42) and at least one local main memory (44) and connected to a local coherence controller (64) including a local cache filter directory SF designed to guarantee local coherence between the local main memory and the cache memories of the module, hereinafter called the local module, each local coherence controller (64) being connected by an external two-point link (55), possibly via a switching device or router (54), to at least one multiprocessor module (51, 52, 53) outside said local module, the coherence controller (64) including a complementary cache filter directory ED for keeping track of the coordinates, particularly

the addresses, of the memory lines or blocks copied from the local module to an external module and guaranteeing coherence between the local main memory (44) and the cache memories (42, 42') of the local module (50) and the external modules (51, 52, 53).

11. Multiprocessor server with a multimodule architecture according to claim 10, characterized in that each coherence controller (64) includes an "n"-bit presence vector (86) designed to indicate the presence or absence of a copy of a memory block or line in the cache memories of the local basic multiprocessors, an "N-1"-bit extension (88) of the presence vector designed to indicate the presence or absence of a copy of a memory block or line in the cache memories of the multiprocessors of the external modules (51, 52, 53) and an Exclusive status bit (87).

12. Multiprocessor server with a multimodule architecture according to claim 10, characterized in that the switching device or router (54) includes means for managing and/or filtering the data and/or requests in transit.